30V, 1A Single Cell Li-Ion & Li-Pol Linear Battery Charger And 20V P-Channel Power MOSFET

General Description

The DS6502 series of devices are highly integrated Li-Ion and Li-Pol linear chargers devices targeted at space-limited portable applications.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination.

The fast charge current value is also programmable via an external resistor.

Features

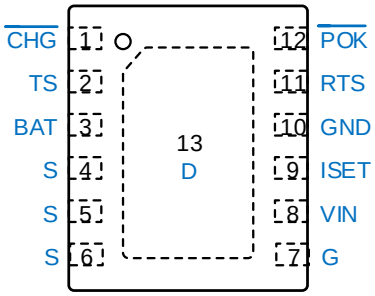
- 30V Input Rating ; with 7.36V Input Overvoltage Protection
- 1% Charge Voltage Accuracy
- Programmable Charger Current 50mA to 1A
- 125°C Thermal Regulation
- Fixed ISET / 5 for Termination of Charge Current
- Fixed ISET / 3 for Pre-Charge Current
- Operation over JEITA Range via Battery NTC – 1/2 Fast-Charge-Current at Cold, 4.05V at Hot
- Adjustable Temperature Sense Current
- Very Low Battery leakage Current 0.1uA
- Prevent Battery Reverse Connection Function
- Built-In P-Channel Power MOSFET
- DFN3x3-12L Package Available

Applications

- Laptop, Palmtops and PDAs
- Smart Phones
- MP3 Players
- Low-Power Handheld Devices
- E-Cig

Pin Configurations

DFN3x3-12L



Ordering Information

DS6502XYY

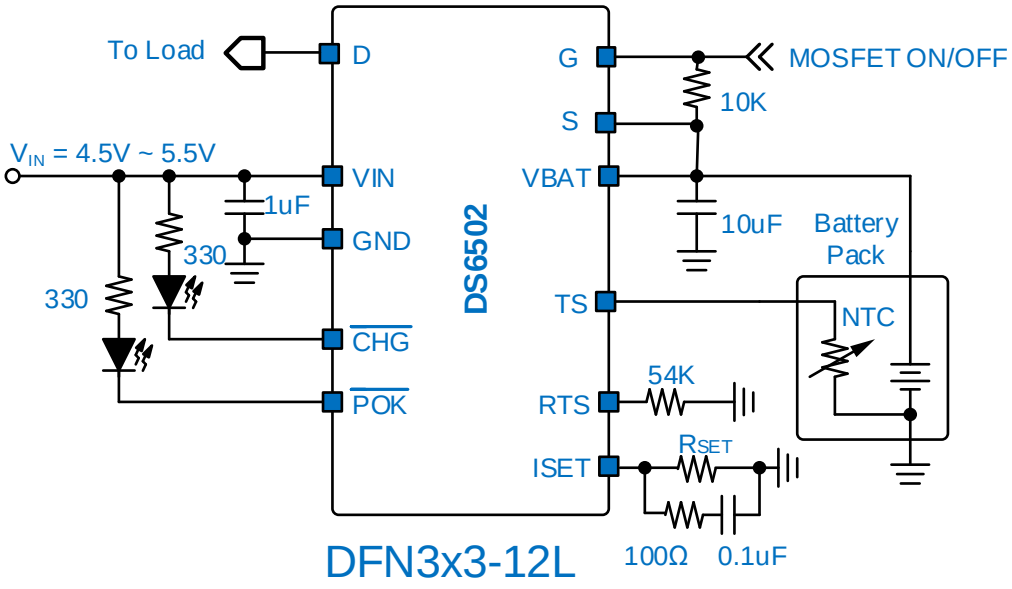
Designator	Description	Symbol	Description
X	V_{BAT}	A	4.2V
		B	4.35V
YY	Package type	D12	DFN3x3-12L

Example: V_{BAT}=4.2V, DFN-3X3-12L. Part no = DS6502AD12

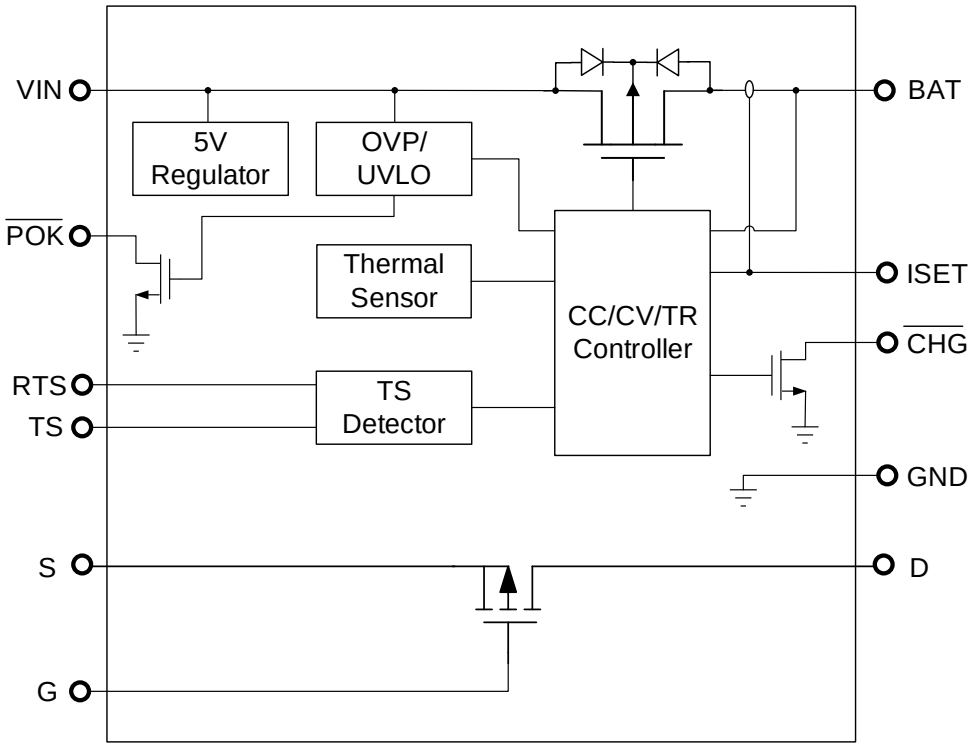
Description of Functional Pins

Pin No DFN-3X3	Pin Name	Pin Function
1	$\overline{CHG}$	Low (FET on) indicates charging and Open Drain (FET off) indicates no Charging or Charge complete.
2	TS	Temperature sense terminal connected to 10k & 100k at 25°C NTC thermistor, in the battery pack. Floating TS terminal or pulling High disables TS monitoring. Pulling terminal Low disables the IC. Let the RTS pin floating if there is no TS requirement.
3	BAT	Battery Connection. System Load may be connected. Expected range of bypass capacitors 10uF to 22uF.
4 , 5 , 6	S	Power MOSFET Source Pin .
7	G	Power MOSFET Gate Pin .
8	VIN	Input of Supply Voltage .
9	ISET	Programs the Fast-charge current setting. External resistor from ISET to VSS defines fast charge current value. Range is 3.74KΩ (300mA) to 530Ω (1000mA) .
10	GND	Ground .
11	RTS	Programs the Temperature Sense (TS) current setting. External resistor from RTS to VSS defines the output current of TS pin. Let the RTS pin floating if there is no TS requirement.
12	$\overline{POK}$	Low (FET on) indicates the input voltage is above UVLO and the OUT (battery) voltage , and less than OVP threshold voltage.
13 (Exposed Pad)	D	Power MOSFET Drain Pin .

Typical Application Circuits



Function Block Diagram



Absolute Maximum Ratings (Note 1)

VIN to GND ---------- -0.3V to 30V

BAT to GND ---------- -0.3V to 12V

D to S ---------- 0V to -20V

G to S ---------- -10V to 10V

Other to GND ---------- -0.3V to 6V

Package Thermal Resistance (Note 2)

DFN3x3-12L, θ_{JA} ---------- 70 °C /W

Lead Temperature (Soldering, 10 sec.) ---------- 260 °C

Junction Temperature ---------- 150 °C

Storage Temperature Range ---------- -60 °C to 150 °C

ESD Susceptibility

HBM ---------- 2KV

MM ---------- 200V

Recommended Operating Conditions

Input Voltage VIN ---------- 4.5V to 30V

Junction Temperature Range ---------- -40 °C to 125 °C

Ambient Temperature Range ---------- -40 °C to 85 °C

Electrical Characteristics

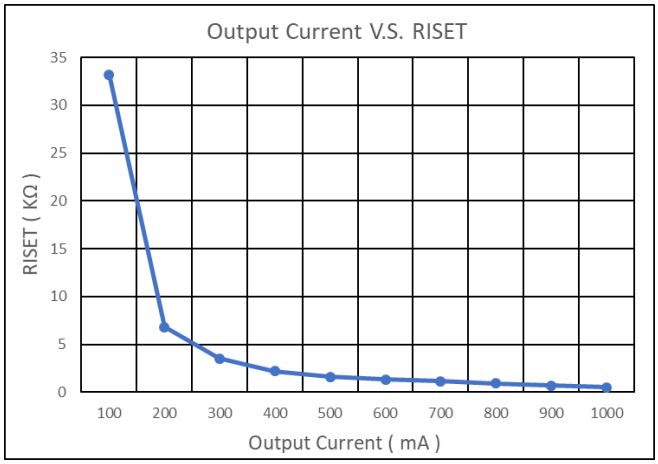
(V_{IN} =5V, T_A=25°C unless otherwise specified)

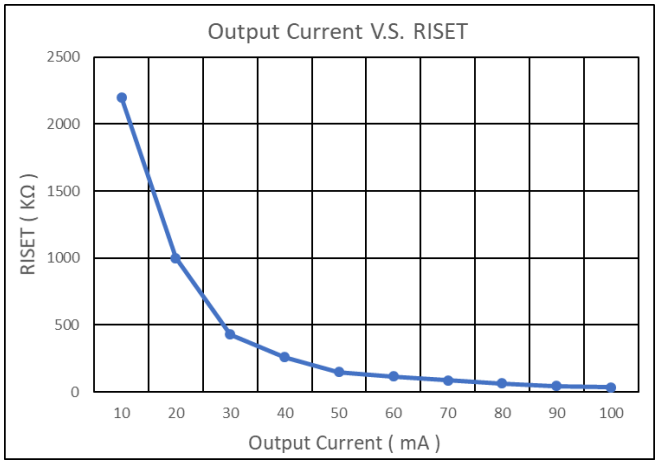
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{IN}		4.6	--	24	V
UVLO Threshold Voltage	V_{IN_UVLO}	V_{IN} Falling	--	4.5	--	V
UVLO Hysteresis Voltage	V_{UVLO_HYS}		--	100	--	mV
Input Over-Voltage Protection	V_{OVP}			7.36		V
Input Over-Voltage Protection Hysteresis	V_{OVP_HYS}			0.1		V
Input Supply Current (Charge mode)	I_{QA}	TS = open, V IN = 5V,no load on OUT terminal,		95		μA
Input Standby Current	I_{QS}	TS = 0V, V IN = 5V		85		μA
Battery leakage current into BAT terminal	I_{BAT}	V_{IN} = 0V, V_{BAT} = 4.2V	--	0.1	--	μA
Reverse Battery Current into BAT terminal	I_{RBAT}	V_{BAT} = -4.2V		800		μA
Battery Regulation Voltage	V_{BAT} / Type A	I_{OUT} = 25mA	4.16	4.2	4.24	V
	V_{BAT} / Type B		4.31	4.35	4.39	
Output Current	I_{OUT}	R_{ISET} = 530 to 124KΩ	50		1000	mA
Pre-charge to fast-charge transition threshold	V_{LOWV}	V_{BAT} Falling	--	2.81	--	V
Temperature Sense Current	I_{TS}	R_{RTS} = 54kΩ	--	100	--	μA
Low temperature CHG Pending	V_{TS}-0°C	TS Rising	--	2.53	--	V
Hysteresis at 0°C	V_{HYS}-0°C		--	60	--	mV
Low temperature, half charge	V_{TS}-10°C	TS Rising	--	1.71	--	V
Hysteresis at 10°C	V_{HYS}-10°C		--	60	--	mV
High temperature at 4.1V	V_{TS}-45°C	TS Falling	--	0.45	--	V
Hysteresis at 45°C	V_{HYS}-45°C		--	17	--	mV
High temperature Disable	V_{TS}-60°C	TS Falling	--	0.28	--	mV
Hysteresis at 60°C	V_{HYS}-60°C		--	17	--	mV
Charge Shutdown Threshold	V_{TS_SD}	TS Falling		110		mV
Hysteresis of TS Shutdown	V_{TS_SD-HYS}			17		mV
Temperature regulation limit	T_J(REG)			125		°C
Thermal shutdown temperature	T_{J_OFF}			155		°C
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V , I_D=-250uA	-20	--	--	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V , I_D=-4A	--	30	--	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS} , I_D=-250uA	-0.3	--	-1.0	V

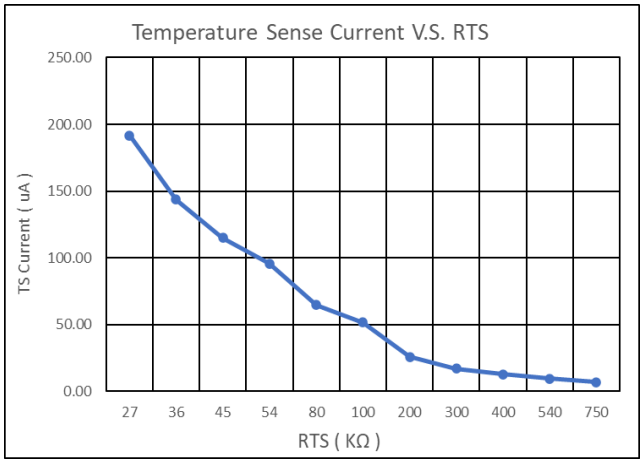
Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

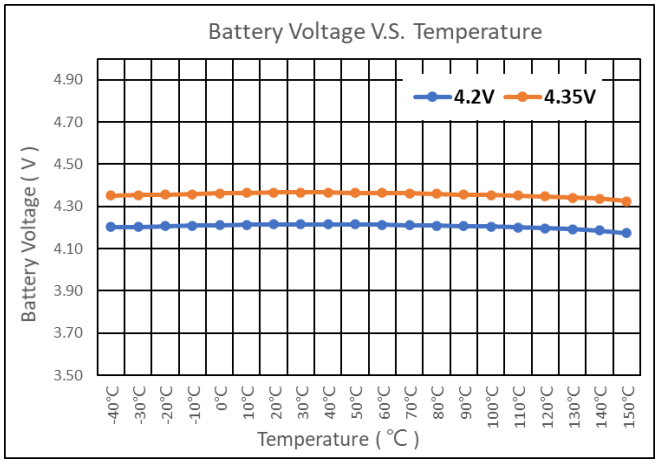
Note 2. θ_{JA} is measured at T_A = 25°C on a DSTECH EVB board.

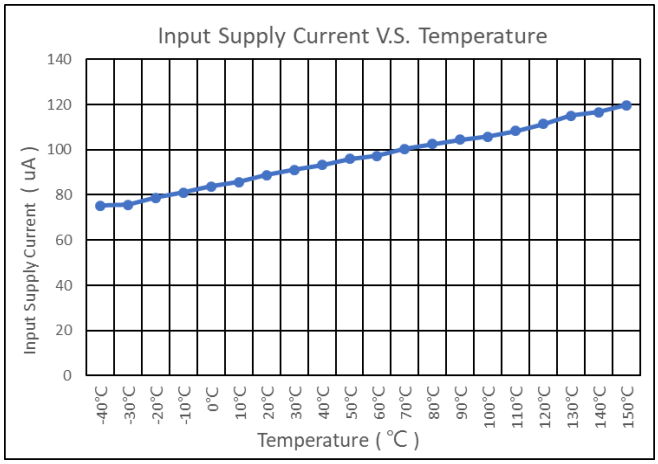
Typical Characteristics

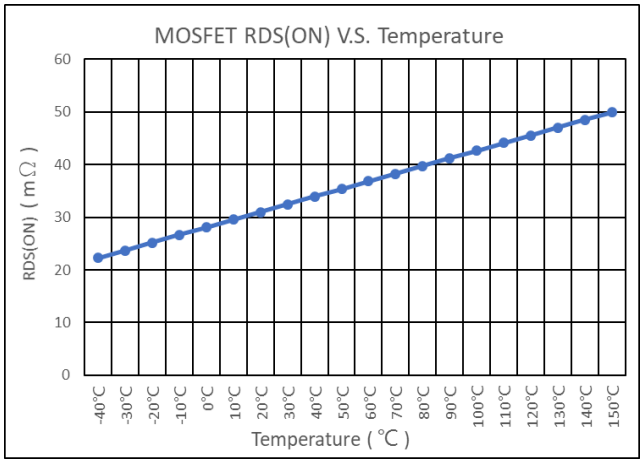












Application Guideline

Power-Down or Undervoltage Lockout (UVLO)

The DS6502 is in power down mode if the VIN terminal voltage is less than UVLO. The part is considered “dead” and all the terminals are high impedance. Once the VIN voltage rises above the UVLO threshold the IC will enter Active mode.

Power-up

The IC is alive after the VIN voltage ramps above UVLO, resets all logic, and starts to perform many of the continuous monitoring routines. Typically, the input voltage quickly rises through the UVLO and declares power good.

Overvoltage-Protection (OVP)

If the input source applies an overvoltage, the pass FET, if previously on, turns off after a deglitch (OVP). The $\overline{CHG}$ and $\overline{POK}$ terminal goes to a high impedance state. Once the overvoltage returns to a normal voltage, the $\overline{POK}$ terminal goes low, charge continues and the $\overline{CHG}$ terminal goes low after a deglitch period.

Program the Temperature Sense Current , RTS

From the Electrical Characteristics table:

RTS (KΩ)	for Battery NTC
54	10K
540	100K

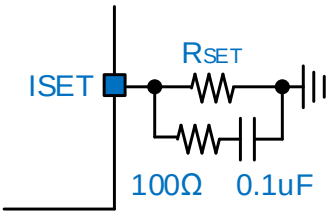
Selecting the closest standard value, use a resistor between RTS and GND.

Program the Fast Charge Current , ISET

From the Electrical Characteristics table:

R_{SET} (KΩ)	Charge Current (mA)
0.536	1000
0.715	900
0.825	800
1.02	700
1.30	600
1.69	500
2.37	400
3.74	300
7.50	200
28.00	100
124.00	50

Selecting the closest standard value, use a R_{SET} resistor between ISET and GND.



It is recommended to connect a set of RC (100Ω & 0.1uF) in parallel with the RSET resistor, which can make the charging current more stable.

$\overline{CHG}$ and $\overline{POK}$ LED Pull-up Source

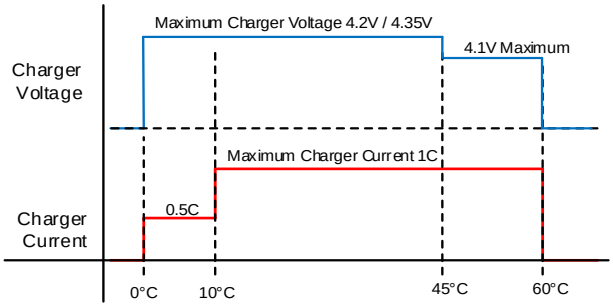
For host monitoring, a pull-up resistor is used between the "STATUS" terminal and the VCC of the host and for a visual indication a resistor in series with an LED is connected between the "STATUS" terminal and a power source. If the $\overline{CHG}$ or $\overline{POK}$ source is capable of exceeding 7V, a 6.2V Zener diode should be used to clamp the voltage. If the source is the BAT terminal, note that as the battery changes voltage, and the brightness of the LEDs vary.

Charging State	$\overline{CHG}$ FET/LED
1st Charge after VIN applied	ON
OVP or UVLO	OFF

VIN Power Good State	$\overline{POK}$ FET/LED
UVLO	OFF
OVP Mode	
Normal Input (UVLO < VIN < V_{OVP})	ON
POK is independent of chip disable	

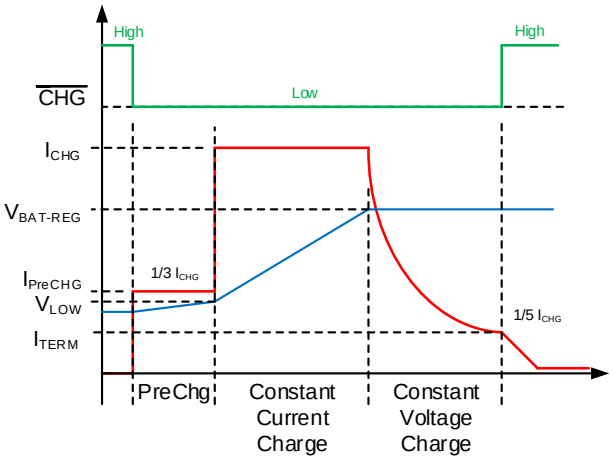
Temperature Sense (TS)

The TS function for the DS6502 is designed to follow the new JEITA temperature standard for Li-Ion and Li-Pol batteries. There are now four thresholds, 60°C, 45°C, 10°C, and 0°C. Normal operation occurs between 10°C and 45°C. If between 0°C and 10°C the charge current level is cut in half and if between 45°C and 60°C the regulation voltage is reduced to 4.1Vmax.



The TS feature is implemented using an internal by RTS set current source to bias the thermistor (designed for use with a 10K NTC β = 4050) connected from the TS terminal to VSS. If this feature is not needed, a fixed 10KΩ can be placed between TS and VSS to allow normal operation. This may be done if the host is monitoring the thermistor and then the host would determine when to pull the TS terminal low to disable charge.

Charge Cycle



Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:

T_A=25°C, DSTECH PCB,

The max PD(Max) = (125°C − 25°C) / (70°C/W) = 1.43W for DFN-12L 3x3 packages.

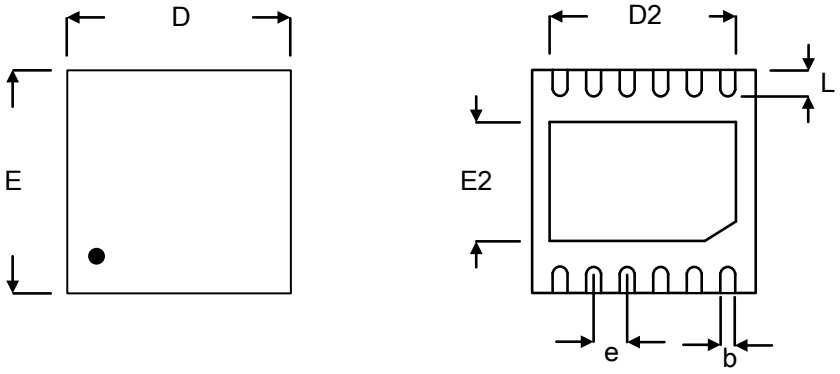
Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

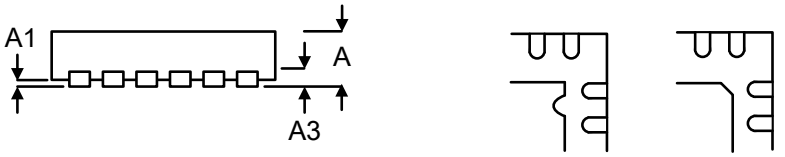
PD = (VIN – VOUT) × IOUT

Layout Consideration

By placing input and output capacitors on the same side of the PCB as the Charger, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the DS6502 ground pin using as wide and as short of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

Package Information:





DETAILA
PIN #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D1	0.260	0.360	0.010	0.014
D2	2.500		0.098	
E	2.900	3.100	0.114	0.122
E2	1.550		0.061	
e	0.450		0.018	
L	0.300	0.500	0.012	0.020

DFN3x3-12L