2μA, 300mA Low Dropout Voltage Linear Regulator

General Description

The DS8561 series are a group of low-dropout (LDO) voltage regulators offering the benefits of wide input voltage range from 1.2V to 5.5V, low dropout voltage, low power consumption, and miniaturized packaging.

Quiescent current of only 2μA makes these devices ideal for powering the battery-powered, always-on systems that require very little idle-state power dissipation to a longer service life. There is an option of shutdown mode by selecting the parts with the EN pin and pulling it low. The shutdown current in this mode goes down to only 10nA (typical).

The DS8561 series of linear regulators are stable with the ceramic output capacitor over its wide input range from 1.2V to 5.5V and the entire range of output load current (0mA to 300mA).

Features

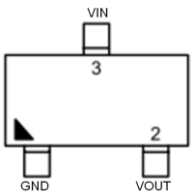
- 2μA Ground Current at no Load
- ±2% Output Accuracy
- 300mA Output Current
- 10nA Disable Current (by option)
- Wide Operating Input Voltage Range: 1.2V to 5.5V
- Dropout Voltage: 0.16V at 300mA/ V_{OUT} 3.3V
- Support Fixed Output Voltage 1.2V, 1.5V, 1.6V, 1.8V, 2.5V, 2.8V, 3.0V, 3.3V
- Stable with Ceramic or Tantalum Capacitor
- Current Limit Protection
- Over-Temperature Protection
- SOT-23-3 , SOT-23-5 , DFN1x1-4L and DFN2x2-6L Packages Available

Applications

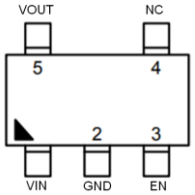
- Portable, Battery Powered Equipment
- Low Power Microcontrollers
- Laptop, Palmtops and PDAs
- Wireless Communication Equipment
- Audio/Video Equipment
- Car Navigation Systems

Pin Configurations

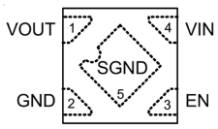
SOT-23-3



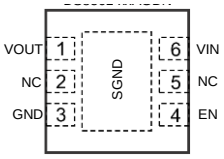
SOT-23-5



DFN1x1-4L



DFN2x2-6L



Ordering Information

DS8561-AABB

Designator	Description	Symbol	Description
AA	Output Voltage	12	V_{OUT} = 1.2V
		..	..
		25	V_{OUT} = 2.5V
		..	..
		33	V_{OUT} =3.3V
		2H	V_{OUT} =2.85V
BB	Package type	S3	SOT-23-3
		S5	SOT-23-5
		D4	DFN1x1-4L
		D6	DFN2x2-6L

Description of Functional Pins

DS8561

Pin No				Pin Name	Pin Function
SOT-23-3	SOT-23-5	DFN1x1	DFN2x2		
1	2	2	3	GND	Ground
2	5	1	1	VOUT	Output of the Regulator
3	1	4	6	VIN	Input of Supply Voltage.
	3	3	4	EN	Enable Control Input.
	4		2,5	NC	No internal connection
		Exposed Pad	Exposed Pad	SGND	Substrate of Chip. Leave floating or tie to GND.

Typical Application Circuit

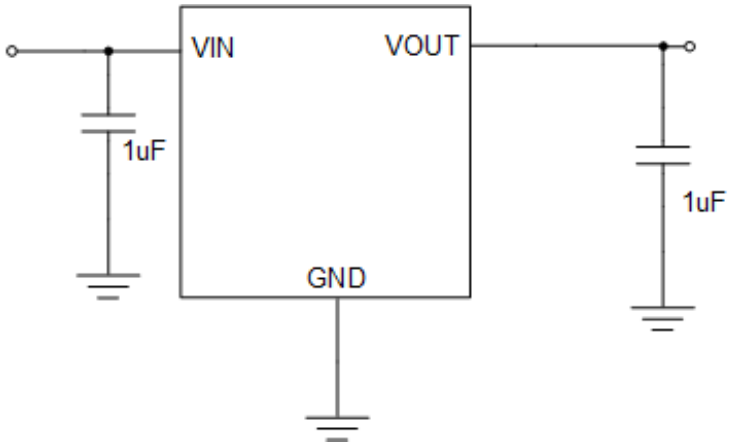


Figure 1: Application circuit of Fixed V_{OUT} LDO

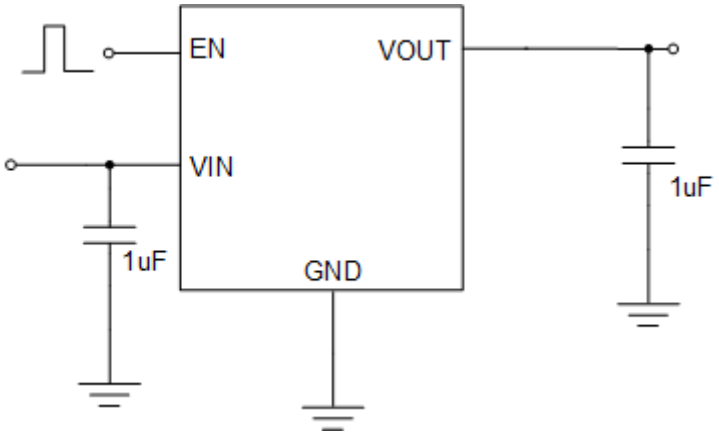
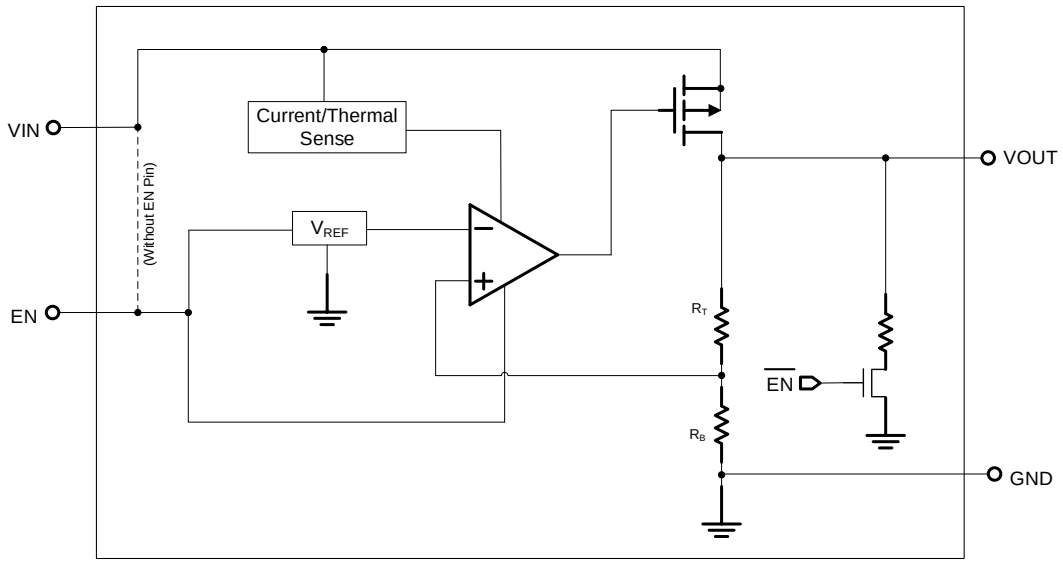


Figure 2: Application circuit of Fixed V_{OUT} LDO with enable function

Function Block Diagram



Absolute Maximum Ratings (Note 1)

VIN to GND ---------- -0.3V to 6.5V

VOUT, EN to GND ---------- -0.3V to 6V

VOUT to VIN ---------- -6V to 0.3V

Package Thermal Resistance (Note 2)

SOT-23-5, SOT-23-3, θ_{JA} ---------- 200 °C /W

DFN1x1-4L, θ_{JA} ---------- 130 °C /W

DFN2x2-6L , θ_{JA} ---------- 95 °C /W

Lead Temperature (Soldering, 10 sec.) ---------- 260 °C

Junction Temperature ---------- 150 °C

Storage Temperature Range ---------- -60 °C to 150 °C

ESD Susceptibility

HBM ---------- 2KV

MM ---------- 200V

CDM ---------- 2KV

Recommended Operating Conditions

Input Voltage VIN ---------- 1.2V to 5.5V

Junction Temperature Range ---------- -40 °C to 125 °C

Ambient Temperature Range ---------- -40 °C to 85 °C

Electrical Characteristics

(V_{IN} =5V, V_{EN} = 5V T_A=25°C unless otherwise specified)

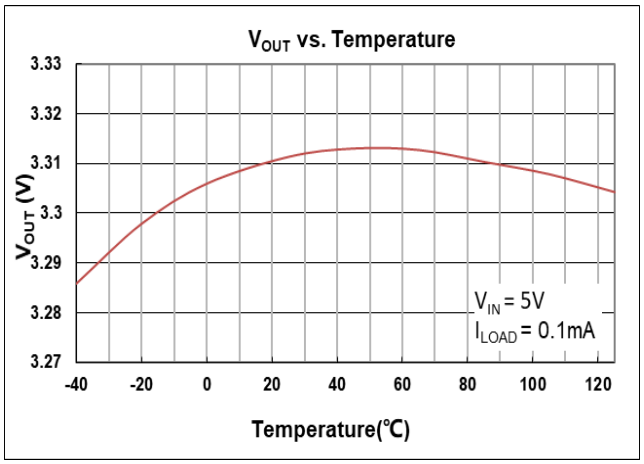
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Voltage	V_{IN}			1.2	--	5.5	V
DC Output Voltage Accuracy		I_{LOAD} =0.1mA		-2		2	%
Dropout Voltage (I_{LOAD} =300mA) (Note 3)	V_{DROP_3V}	V_{OUT} ≥ 3V			0.16		V
	$V_{DROP\_2.8V}$	V_{OUT} = 2.8V			0.18		
	$V_{DROP\_2.5V}$	V_{OUT} = 2.5V			0.2		
	$V_{DROP\_1.8V}$	V_{OUT} = 1.8V			0.25		
	$V_{DROP\_1.5V}$	V_{OUT} = 1.5V			0.31		
	$V_{DROP\_1.2V}$	V_{OUT} = 1.2V			0.41		
Ground Current	I_Q	I_{LOAD} = 0mA			2		μA
Shutdown Ground Current	I_{SD}	V_{EN} = 0V,			0.01	0.5	μA
V_{OUT} Shutdown Leakage Current	I_{LEAK}	V_{OUT} = 0V			0.01	0.5	
Enable Threshold Voltage	V_{IH}	EN Rising				2	V
	V_{IL}	EN Falling		0.6			
EN Input Current	I_{EN}	V_{EN} = 5V			10	100	nA
Line Regulation	ΔLINE	I_{LOAD} =30mA, 1.5V ≤ V_{IN} ≤ 5.5V or (V_{OUT} + 0.2V) ≤ V_{IN} ≤ 5.5V			0.2		%
Load Regulation	ΔLOAD	10mA ≤ I_{LOAD} ≤ 0.3A			0.2		%
Output Current Limit	I_{LIM}	V_{OUT} =0		301	600		mA
Power Supply Rejection Ratio (I_{LOAD} =5mA)	PSRR	V_{OUT} =1.2V, V_{IN} = 2V	f = 100Hz	--	80	--	dB
			f = 1kHz	--	75	--	
Output Voltage Noise (BW = 10Hz to 100kHz, C_{OUT} =1μF,)		V_{IN} = 3.5V I_{LOAD} =0.1A	V_{OUT} =0.9V	--	40	--	μV_{RMS}
			V_{OUT} =2.8V	--	50	--	
Thermal Shutdown Temperature	T_{SD}	I_{LOAD} =10mA		--	155	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}			--	15	--	°C
Discharge Resistance		EN = 0V , V_{OUT} = 0.1V		--	100	--	Ω

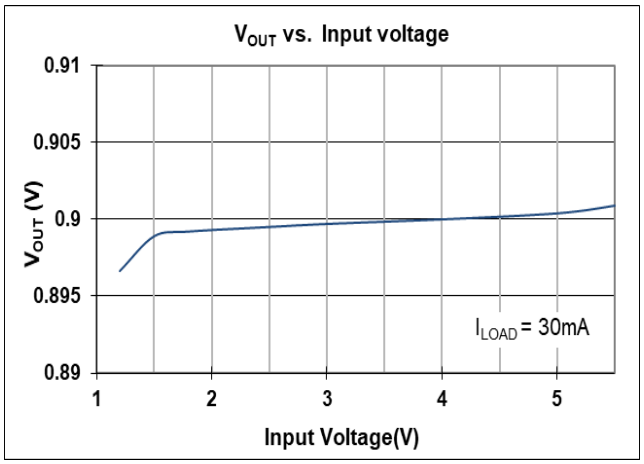
Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

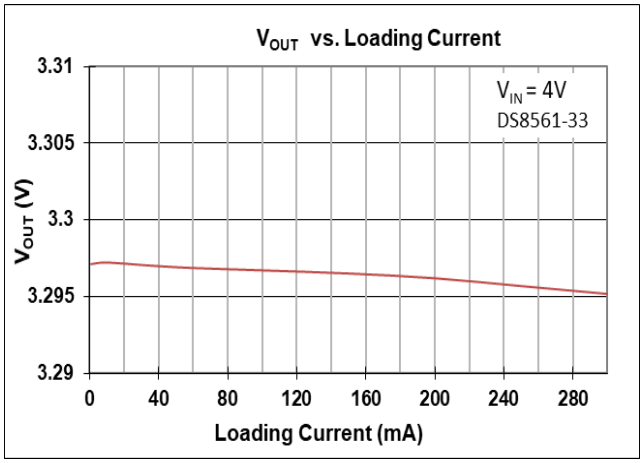
Note 2. θ_{JA} is measured at T_A = 25°C on a DSTECH EVB board.

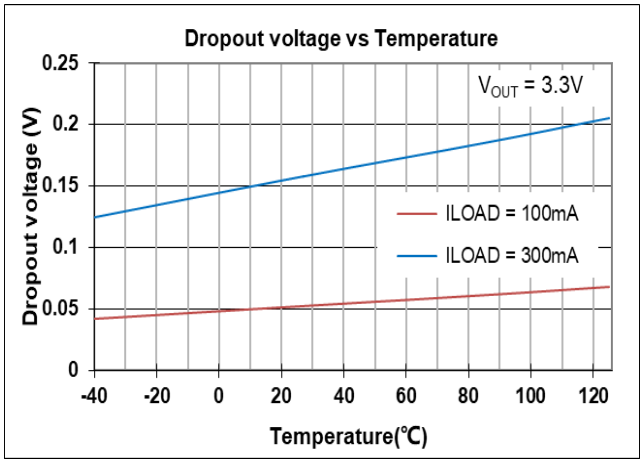
Note 3. $V_{DROP} = V_{IN} - V_{OUT}$ when the V_{OUT} is 98% of its target value.

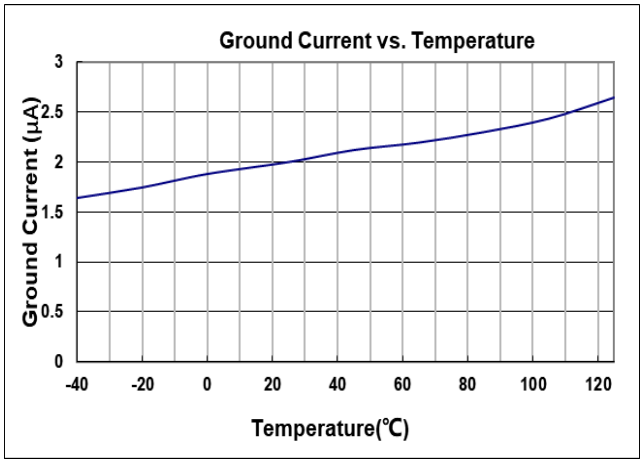
Typical Characteristics

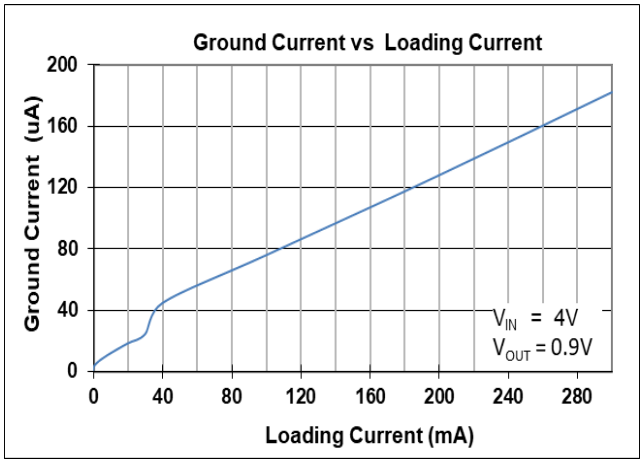


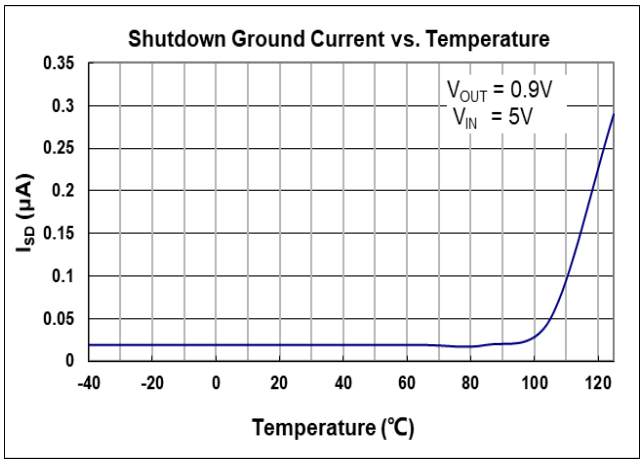


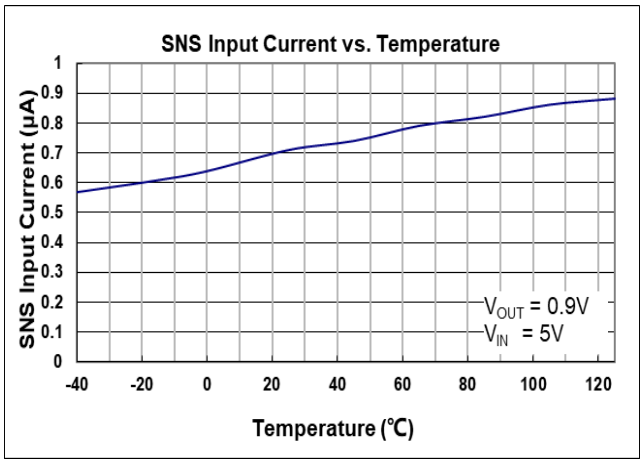


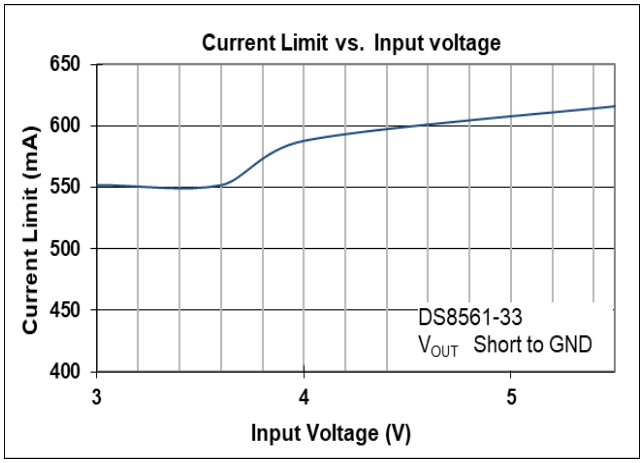




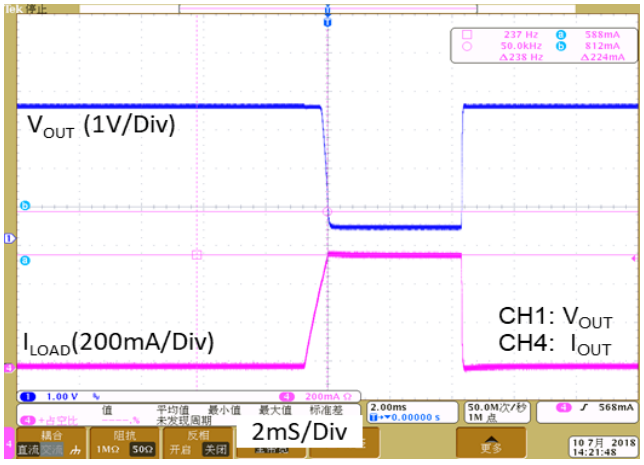




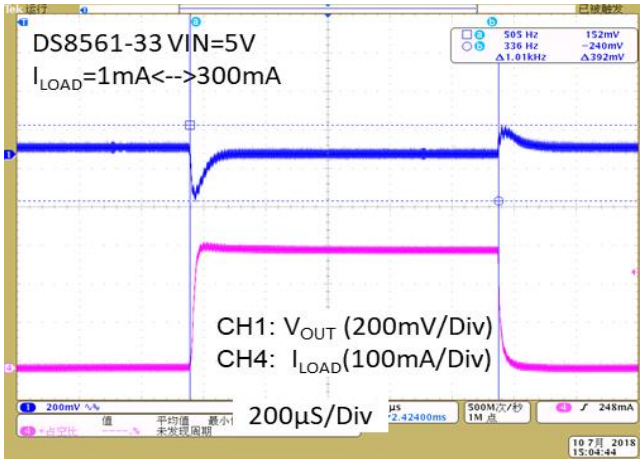




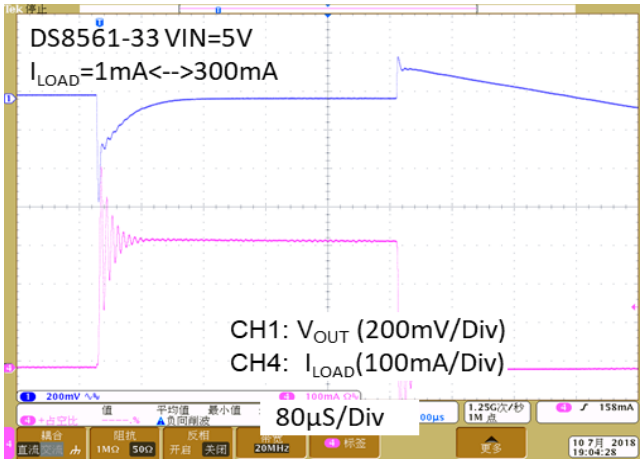
Current Limit Response



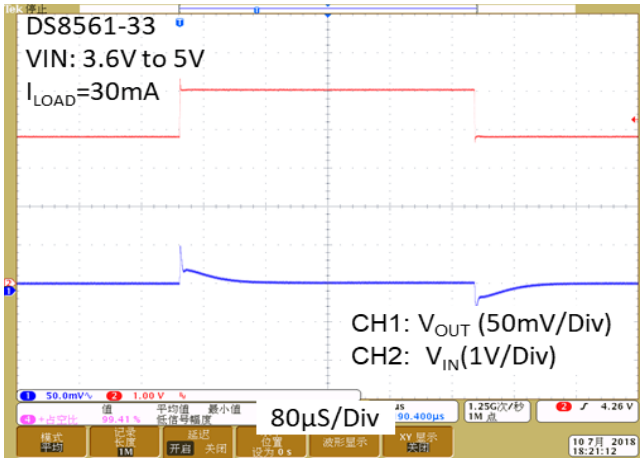
Load Transient Response I



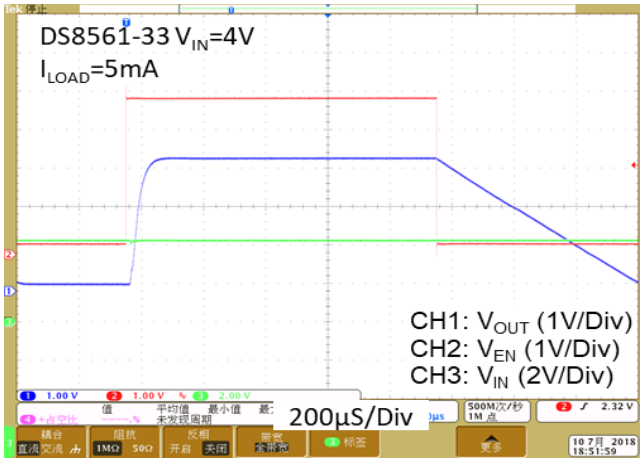
Load Transient Response II



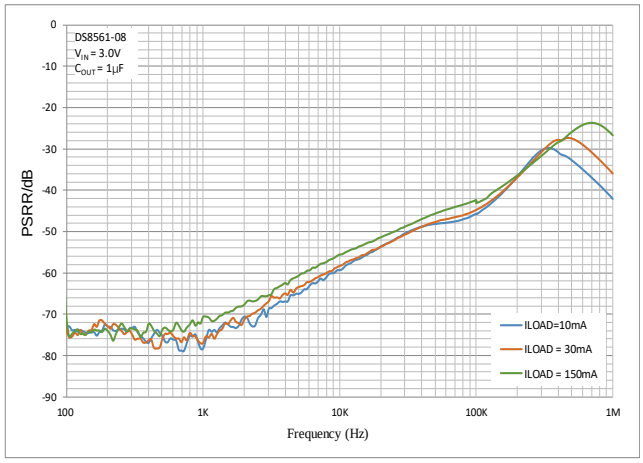
Line Transient Response



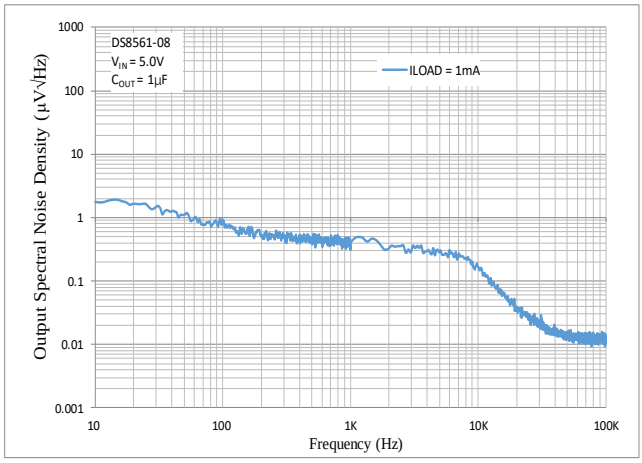
V_{OUT} Turn On/Off by EN



PSRR vs. Frequency



Noise Density Spectrum



Application Guideline

Input and Output Capacitor Requirements

The external input and output capacitors of DS8561 series must be properly selected for stability and performance. Use a 1μF or larger input capacitor and place it close to the IC's V_{IN} and GND pins. Any output capacitor meeting the minimum 1mΩ ESR (Equivalent Series Resistance) and effective capacitance between 1μF and 22μF requirement may be used. Place the output capacitor close to the IC's V_{OUT} and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

Current Limit

The DS8561 series contain the current limiter of output power transistor, which monitors and controls the transistor, limiting the output current to 600mA (typical). The output can be shorted to ground indefinitely without damaging the part.

Dropout Voltage

The DS8561 series use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DROP}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $RDS_{(ON)}$ of the PMOS pass element. V_{DROP} scales approximately with the output current because the PMOS device behaves as a resistor in dropout condition.

As any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout condition.

OTP (Over Temperature Protection)

The over temperature protection function of DS8561 series will turn off the P-MOSFET when the junction temperature exceeds 155°C (typ.). Once the junction temperature cools down by approximately 15°C, the regulator will automatically resume operation.

Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:

T_A=25°C, DS-Tech PCB,

The max PD (Max) = (125°C − 25°C) / (200°C/W) = 0.5W for SOT-23-3 / SOT-23-5 packages.

The max PD (Max) = (125°C − 25°C) / (130°C/W) = 0.77W for DFN1x1-4L package.

The max PD (Max) = (125°C − 25°C) / (95°C/W) = 1.05W for DFN2x2-6L package.

Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

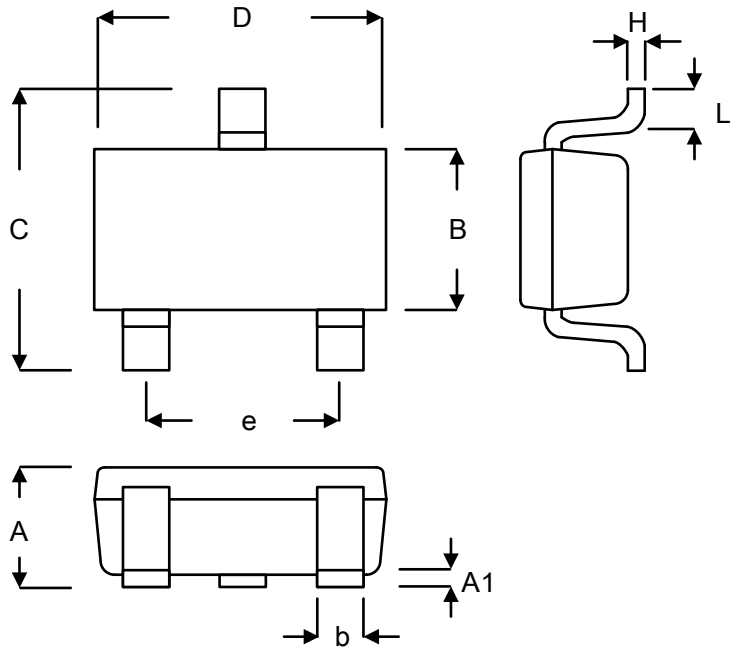
PD = (VIN – VOUT) × IOUT

Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the DS8561 ground pin using as wide and as short of a copper trace as is practical.

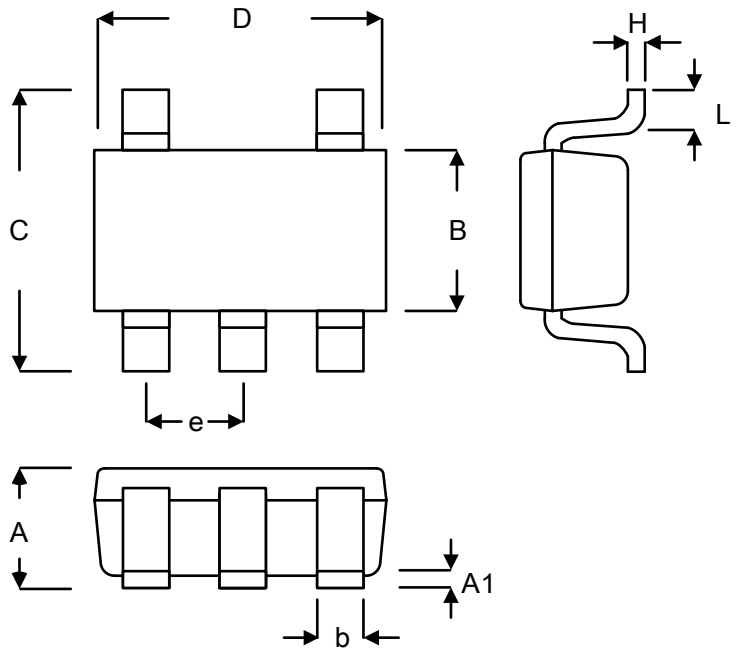
Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

Package Information:



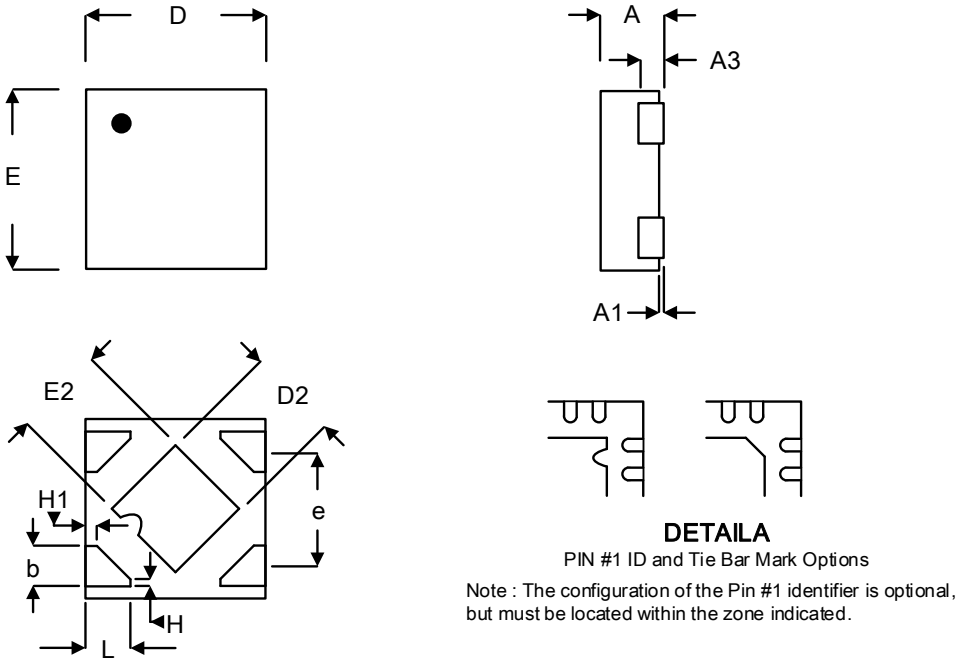
Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	1.803	2.007	0.071	0.079
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-3L



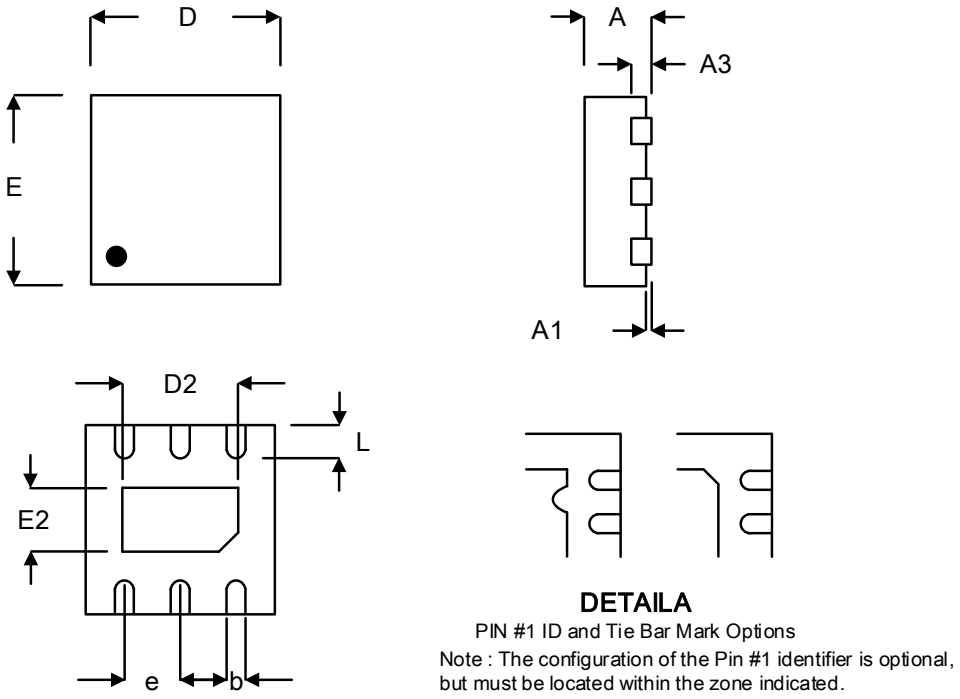
Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5L



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.300	0.400	0.012	0.016
A1	0.000	0.050	0.000	0.002
A3	0.117	0.162	0.005	0.006
b	0.175	0.280	0.007	0.011
D	0.900	1.100	0.035	0.043
D2	0.430	0.550	0.017	0.022
E	0.900	1.100	0.035	0.043
E2	0.430	0.550	0.017	0.022
e	0.650		0.026	
L	0.200	0.300	0.008	0.012
H	0.039		0.002	
H1	0.064		0.003	

DFN1x1-4L



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

DFN2x2-6L