High Voltage Synchronous Rectified Buck MOSFET Driver for Notebook Computer

General Description

The DS9601 is a high frequency, dual MOSFET driver specifically designed to drive two power N-MOSFETS in a synchronous-rectified buck converter topology.

It is especially suited for mobile computing applications that require high efficiency and excellent thermal performance. This driver, combined with multi-phase Buck PWM controllers, provides a complete core voltage regulator solution for advanced micro processors.

The drivers are capable of driving a 3nF load with fast rising/falling time and fast propagation delay. This device implements bootstrapping on the upper gates with only a single external capacitor. This reduces implementation complexity and allows the use of higher performance, cost effective, N-MOSFETs. Adaptive shoot through protection is integrated to prevent both MOSFETs from conducting simultaneously.

The DS9601 is available in DFN2x2-8L Package.

Features

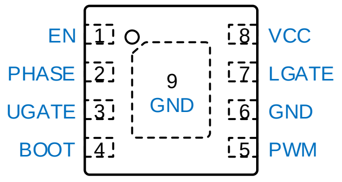
- Drives Two N-MOSFETs
- Adaptive Shoot-Through Protection
- 0.5Ω On-Resistance, 4A Sink Current Capability
- Supports High Switching Frequency
- Tri-State PWM Input for Power Stage Shutdown
- Output Disable Function
- Integrated Boost Switch
- Low Bias Supply Current
- VCC POR Feature Integrated
- DFN2x2-8L Package Available

Applications

- Notebook PC Applications
- Core Voltage Supplies for Intel / AMD Mobile Microprocessors
- High Frequency Low Profile DC/DC Converters
- High Current Low Output Voltage DC/DC Converters
- High Input Voltage DC/DC Converters

Pin Configurations

DFN2x2-8L



Ordering Information

DS9601XX

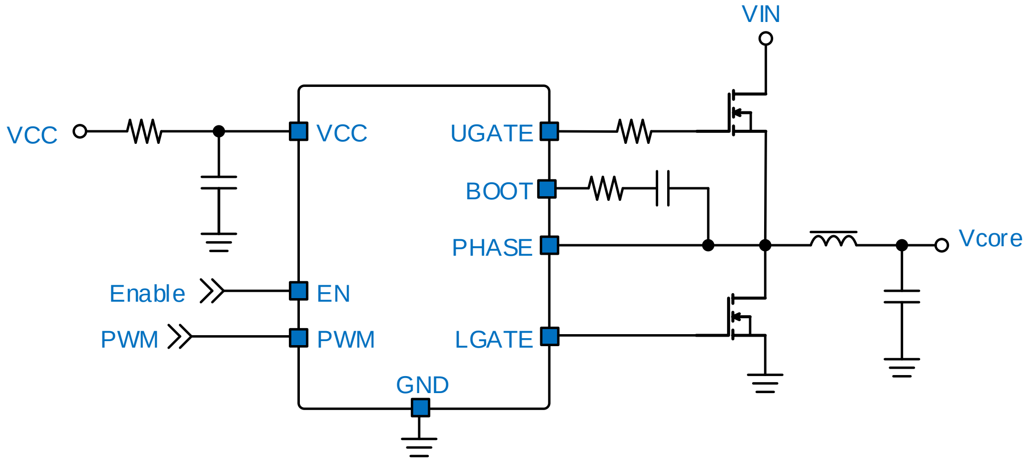
Designator	Description	Symbol	Description
X X	Package type	D8	DFN2x2-8L

Example: DFN2x2-8L. Part no = DS9601D8

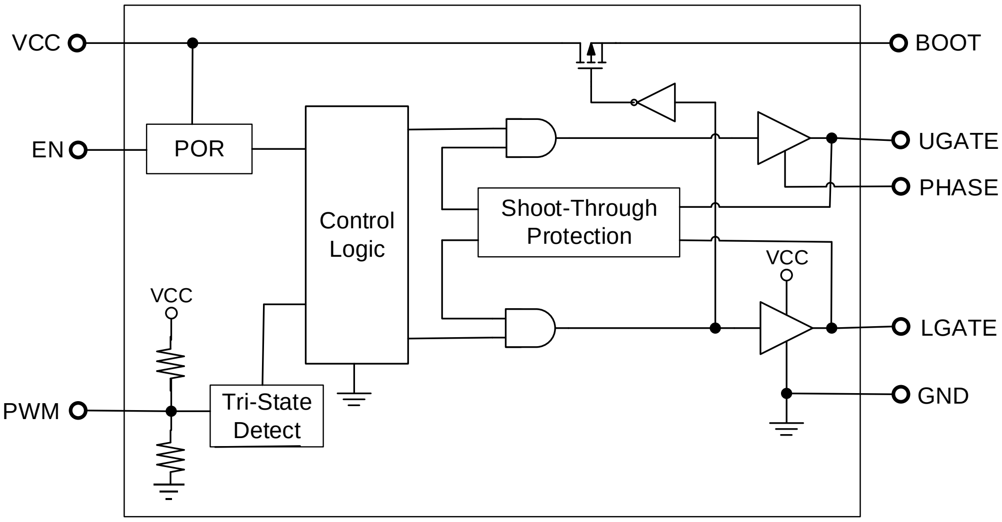
Description of Functional Pins

Pin No	Pin Name	Pin Function
DFN2x2-8L		
1	EN	Enable Pin. When low, both UGATE and LGATE are driven low and the normal operation is disabled.
2	PHASE	Switch Node. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate driver.
3	UGATE	Upper Gate Drive Output. Connect to the gate of high side power N-MOSFET.
4	BOOT	Floating Bootstrap Supply Pin for Upper Gate Drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.
5	PWM	Control Input for Driver. The PWM signal can enter three distinct states during operation. Connect this pin to the PWM output of the controller.
6	GND	Ground.
7	LGATE	Lower Gate Drive Output. Connect to the gate of the low side power N-MOSFET.
8	VCC	Input Supply Pin. Connect this pin to a 5V bias supply. Place a high quality bypass capacitor from this pin to GND.
9 Exposed Pad	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Typical Application Circuits



Function Block Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage, VCC ---------- 0.3V to 6V

BOOT to PHASE ---------- 0.3V to 6V

PHASE to GND

DC ---------- 0.3V to 32V

< 20ns ---------- 8V to 38V

UGATE to PHASE

DC ---------- 0.3V to 6V

< 20ns ---------- 5V to 7.5V

LGATE to GND

DC ---------- 0.3V to 6V

< 20ns ---------- 2.5V to 7.5V

PWM, EN to GND ---------- 0.3V to 6V

Package Thermal Resistance (Note 2)

DFN2x2-8L , θ_{JA} ---------- 48 °C /W

DFN2x2-8L , θ_{JC} ---------- 13 °C /W

Lead Temperature (Soldering, 10 sec.) ---------- 260 °C

Junction Temperature ---------- 150 °C

Storage Temperature Range ---------- -60 °C to 150 °C

ESD Susceptibility

HBM ---------- 2KV

MM ---------- 200V

Recommended Operating Conditions

Input Voltage VIN ---------- 4.5V to 26V

Control Voltage, VCC ---------- 4.5V to 5.5V

Junction Temperature Range ---------- -40 °C to 125 °C

Ambient Temperature Range ---------- -40 °C to 85 °C

Electrical Characteristics

(VCC = 5V, C_{IN} = C_{OUT} = 10uF, C_{VCC} = 1uF, T_A = 25℃, unless otherwise specified)

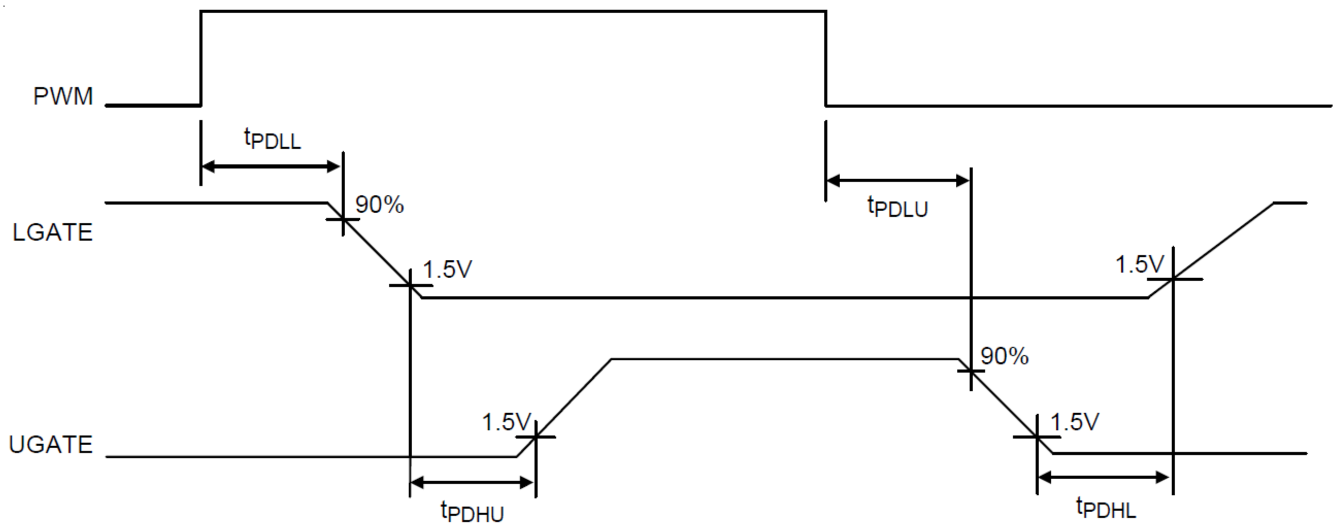
Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VCC Supply Current							
Quiescent Current		I_Q	PWM Pin Floating, V_{EN} = 3.3V	--	80	--	uA
Shutdown Current		I_{SHDN}	V_{EN} = 0V, PWM = 0V, V_{CC} = 5V	--	0	5	uA
VCC Power On Reset (POR)		V_{PORH}	VCC POR Rising	--	4.2	4.5	V
		V_{PORL}	VCC POR Falling	3.5	3.84	--	V
		V_{PORHYS}	Hysteresis	--	360	--	mV
Internal BOOT Switch							
Internal Boost Switch On Resistance		R_{BOOT}	VCC to BOOT, 10mA	--	--	80	Ω
PWM Input							
Input Current		I_{PWM}	V_{PWM} = 5V	--	150	--	uA
			V_{PWM} = 0V	--	-150	--	
PWM Tri-State Rising Threshold		V_{PWMH}	VCC = 5V	3.5	3.8	4.1	V
PWM Tri-State Falling Threshold		V_{PWML}	VCC = 5V	0.7	1	1.3	V
EN Input							
EN Input Voltage	Logic-High	V_{ENH}	VCC = 5V	2	--	--	V
	Logic-Low	V_{ENL}	VCC = 5V	--	--	0.48	
Switching Time							
UGATE Rise Time		t_{UGATEr}	VCC = 5V, 3nF Load	--	8	--	ns
UGATE Fall Time		t_{UGATEf}	VCC = 5V, 3nF Load	--	8	--	ns
LGATE Rise Time		t_{LGATEr}	VCC = 5V, 3nF Load	--	8	--	ns
LGATE Fall Time		t_{LGATEf}	VCC = 5V, 3nF Load	--	4	--	ns
UGATE Turn-Off Propagation Delay		t_{PDLU}	VCC = 5V, Outputs Unloaded	--	35	--	ns
LGATE Turn-Off Propagation Delay		t_{PDLL}	VCC = 5V, Outputs Unloaded	--	35	--	ns
UGATE Turn-On Propagation Delay		t_{PDHU}	VCC = 5V, Outputs Unloaded	--	20	--	ns
LGATE Turn-On Propagation Delay		t_{PDHL}	VCC = 5V, Outputs Unloaded	--	20	--	ns
UGATE/LGATE Tri-State Propagation Delay		t_{PTS}	VCC = 5V, Outputs Unloaded	--	35	--	ns

Output						
UGATE Driver Source Resistance	$R_{UGATEsr}$	100mA Source Current	--	1	--	Ω
UGATE Driver Source Current	$I_{UGATEsr}$	VUGATE - VPHASE = 2.5V	--	2	--	A
UGATE Driver Sink Resistance	$R_{UGATEsk}$	100mA Sink Current	--	1	--	Ω
UGATE Driver Sink Current	$I_{UGATEsk}$	VUGATE - VPHASE = 2.5V	--	2	--	A
LGATE Driver Source Resistance	$R_{LGATEsr}$	100mA Source Current	--	1	--	Ω
LGATE Driver Source Current	$I_{LGATEsr}$	VLGATE = 2.5V	--	2	--	A
LGATE Driver Sink Resistance	$R_{LGATEsk}$	100mA Sink Current	--	0.5	--	Ω
LGATE Driver Sink Current	$I_{LGATEsk}$	VLGATE = 2.5V	--	4	--	A

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a DSTECH EVB board.

Timing Diagram



Application Guideline

Supply Voltage and Power On Reset

The DS9601 is designed to drive both high side and low side N-MOSFETs through an externally input PWM control signal. Connect 5V to VCC to power on the DS9601. A minimum 1uF ceramic capacitor is recommended to bypass the supply voltage. Place the bypassing capacitor physically near the IC. The power on reset (POR) circuit monitors the supply voltage at the VCC pin. If VCC exceeds the POR rising threshold voltage, the controller resets and prepares for operation. UGATE and LGATE are held low before VCC is above the POR rising threshold.

Enable and Disable

The DS9601 includes an EN pin for sequence control. When the EN pin rises above the VENH trip point, the DS9601 begins a new initialization and follows the PWM command to control the UGATE and LGATE. When the EN pin falls below the VENL trip point, the DS9601 shuts down and keeps UGATE and LGATE low.

Three State PWM Input

After initialization, the PWM signal takes over the control. The rising PWM signal first forces the LGATE signal low and then allows the UGATE signal to go high right after a non-overlapping time to avoid shoot through current. In contrast, the falling PWM signal first forces UGATE to go low. When the UGATE or PHASE signal reach a predetermined low level, LGATE signal is then allowed to go high.

Non-overlap Control

To prevent the overlap of the gate drives during the UGATE pull low and the LGATE pull high, the non-overlap circuit monitors the voltages at the PHASE node and high side gate drive (UGATE-PHASE). When the PWM input signal goes low, UGATE begins to pull low (after propagation delay). Before LGATE can pull high, the non-overlap protection circuit ensures that the monitored (UGATE- PHASE) voltages have gone below 1.1V and phase voltage is below 2V. Once the monitored voltages fall below the threshold, LGATE begins to turn high. By waiting for the voltages of the PHASE pin and high side gate drive to fall below their threshold, the non-overlap protection circuit ensures that UGATE is low before LGATE pulls high.

Also to prevent the overlap of the gate drives during LGATE pull low and UGATE pull high, the non-overlap circuit monitors the LGATE voltage. When LGATE go below 1.1V, UGATE is allowed to go high.

Driving Power MOSFETs

The DC input impedance of the power MOSFET is extremely high. The gate draws the current only for few nano-amperes. Thus once the gate has been driven up to “ON” level, the current could be negligible.

However, the capacitance at the gate to source terminal should be considered. It requires relatively large currents to drive the gate up and down rapidly. It is also required to switch drain current on and off with the required speed. The required gate drive currents are calculated as follows.

Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:

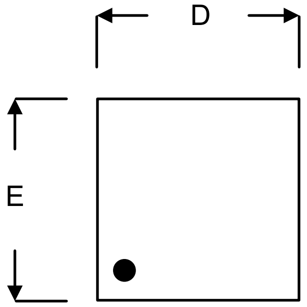
T_A=25°C, DSTECH PCB,

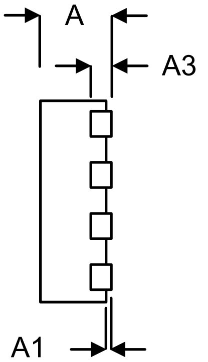
The max PD(Max) = (125°C − 25°C) / (48°C/W) = 2.08W for DFN2x2-8L packages.

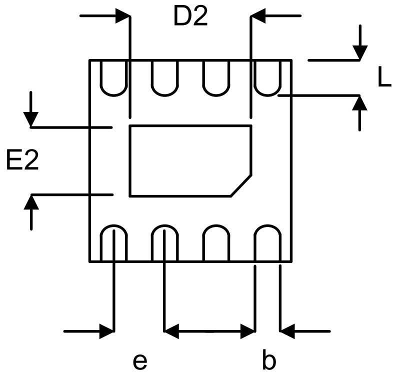
Layout Consideration

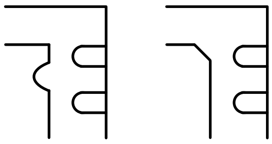
By placing input and output capacitors on the same side of the PCB as the Charger, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the DS9601 ground pin using as wide and as short of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

Package Information:









DETAILA

PIN #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203		0.008	
b	0.200	0.300	0.008	0.012
D	1.900	2.100	0.075	0.083
D2	1.200		0.047	
E	1.900	2.100	0.075	0.083
E2	0.700		0.028	
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

DFN2x2-8L